REMARKS

This Amendment is in response to the Final Office Action mailed 9/4/2003 and Advisory Action mailed 2/2/2004. Applicant has filed a Request for Continued Examination to have the Office withdraw the finality of the Office Action and have this submission entered and considered.

Invitation to Copy Claims

In the Office Action mailed June 10, 2003, the Examiner issued an invitation to copy a claim under 37 CFR § 1.605 for the purpose of an interference with Ryan (US 6,449,679) as follows:

A processing system comprising:

a memory controller that issues and receives commands in a packet based RDRAM protocol;

a plurality of memory modules comprising SDRAM devices; and

a single interface device located with the memory controller such that the interface device is not located on the memory modules, the interface device translates packet based RDRAM protocol command and data signals from the memory controller into an SDRAM protocol, and the interface device translates data signals received from the memory module into packet based RDRAM protocol data.

Applicant respectfully refused the invitation to copy claims because applicant disagrees that the invention being claimed by the applicant is the same patentable invention as that in the claim suggested by the Examiner.

The following is a quotation of 37 CFR § 1.601(n) that defines "same invention."

> (n) Invention "A" is the same patentable invention as an invention "B" when invention "A" is the same as (35 U.S.C. 102) or is obvious (35 U.S.C. 103) in view of invention "B" assuming invention "B" is prior art with respect to invention "A". Invention "A" is a separate patentable invention with respect to invention "B" when invention "A" is new (35 U.S.C. 102) and non-obvious (35 U.S.C. 103) in view of invention "B" assuming invention "B" is prior art with respect to invention "A".

For the invention claimed by the applicant (invention "A") to be the same invention as that claimed by Ryan (invention "B"), applicant's invention must be the same as (35 U.S.C. 102) or obvious (35 U.S.C. 103) in view of the invention of Ryan assuming the invention of Ryan is prior art with respect to applicant's invention. The Examiner has rejected applicant's claims under 35 U.S.C. § 102(e) as being anticipated by Ryan. Therefore the Examiner is alleging that the invention claimed by the applicant is the same invention as that claimed by Ryan and that Ryan has disclosed and claimed each and every element claimed by the applicant. Applicant respectfully submits that this is not the case.

The claim suggested by the Examiner includes the element of "a packet based RDRAM protocol." Applicant's claims include the element of "a memory control packet." The Examiner

appears to understand these two elements as being equivalent. Applicant respectfully submits that they are patentably distinct.

In the advisory action mailed 2/2//2004 the Examiner stated, "Applicant's reliance on the strict interpretation given to 'Memory Control Packet' is not warranted in light of other language in the specification." Applicant respectfully requests that the Examiner specifically identify the other language in the specification referred to.

As disclosed by Ryan, "a packet based RDRAM protocol" is a packet protocol defined for use with RAMBUS DRAM (RDRAM) memory by RAMBUS, Inc., Mountain View, Calif. Ryan, col. 1, lines 46-47; col. 4, lines 14-26. The packet based RDRAM protocol includes row packets and column packets. Ryan, col. 5, lines 27-61; Direct RDRAM™ 128/144-Mbit, Document DL0059, page 6 (included with Information Disclosure Statement on August 22, 2003).

In contrast, "[memory control packets] utilize a protocol defined by the invention for the purpose of accessing SDRAM memory through the memory channel." Specification, page 9, lines 7-8. Applicant respectfully submits that "memory control packet" had no generally accepted meaning by those skilled in the art at the time of the invention. Therefore, it is necessary to look to applicant's specification to understand what "a memory control packet" reads on. Applicant submits that "a memory control packet" does not read on a packet from a packet based RDRAM protocol as used by Ryan.

A memory control packet contains 32 bits. Specification, page 10, line 21, through page 11, line 1. The RDRAM protocol includes 40 bit COLx packets and a 24 bit ROWx packets. Ryan, col. 5, lines 27-61; Direct RDRAM™ 128/144-Mbit, Document DL0059, page 6. The usage of the bits within these packets to provide command information is entirely different between the memory control packets and the packets of the RDRAM protocol.

Since applicant does not believe that applicant's claimed invention is the same as the invention of the claim suggested by the Examiner for copying, applicant has refused the Examiner's invitation to copy the claim suggested by the Examiner.

Rejection of Claims 1-23

The Examiner rejects claims 1-23 under 35 U.S.C. § 102(e) as being anticipated by either Ryan (US 2001/0042163 A1) or Ryan (US 6,449, 679 B2).

This rejection is traversed on the same basis as discussed above regarding the copying of claims, namely that nothing in Ryan discloses "a memory control packet" as claimed. In considering this argument presented in the previous Response, the Examiner found the argument regarding the difference of the memory control protocol not persuasive because the Examiner considered that "this distinction is conspicuously absent from the claims." As explained above, applicant considers that the term "memory control packet" is defined by the specification and does bring the distinction into the claims. Further, applicant considers that many of the dependent claims include further distinctions between the types of packets processed by the

applicant's invention and the device disclosed by Ryan that have not been fully considered by the Examiner.

The Examiner argues that applicant's claimed invention does exactly what the Ryan reference does. The Examiner then asserts, "Thus, the claims are anticipated." Applicant respectfully reminds the Examiner that identity of what an invention does is not the test of anticipation. To anticipate an invention a reference must disclose each and every element of the invention. Even if the Ryan reference did do exactly what applicant's claimed invention does, which it does not, Ryan would need to do it in the way claimed, using the claimed structures, to anticipate applicant's invention. This Ryan does not do.

Regarding claims 1, 13, and 20, each of these independent claims includes elements for receiving and acting on a memory control packet. Ryan does not disclose any elements for receiving and acting on a memory control packet.

To further distinguish the present invention from the invention of Ryan, applicant has amended claims 1, 13, and 17 to add the further element of timing the transmission of packets on the channel based on the memory bus cycle time as disclosed in the specification as filed on page 9, lines 14-16. Packets of the RDRAM protocol are transmitted without reference to a memory bus cycle time because the Direct RAMBUS™ architecture does not provide a memory bus.

Regarding claims 2-10, 14-16, and 21, asserts that these claims are directed to the physical structure of the RAMBUS memory channel, which is well known and disclosed by Ryan. Applicant respectfully submits that many of these claims are directed to specific aspects of the memory control packet which are not part of the physical structure of the RAMBUS memory channel and which are not disclosed by Ryan. The dependent claims were addressed more specifically in the Office Action mailed on December 24, 2002, which the Examiner has incorporated into the most recent Office Action by reference. In that Office Action only Ryan (US 2001/0042163 A1) was cited and the reference to Ryan in the following remarks are to the published application.

Regarding claims 2 and 14, the examiner asserts that Ryan discloses the memory channel interface receiving a memory control packet only from the control portion of the memory channel, citing fig. 4, els. 8 and 16. Applicant believes the Examiner inadvertently mistook the indications of bus widths to be reference numerals and that element 144 and the element labeled "DQA0-DQA7 DQB0-DQB7" were the intended citations. Applicant respectfully submits that element 144 is the control portion of the memory channel and that nothing in Ryan discloses receiving a memory control packet on the control portion because Ryan does not disclose receiving a memory control packet.

Regarding claim 3, the Examiner asserts that Ryan discloses that the memory control packet includes command flag bits that indicate that the memory control packet is one of an activate command, a read/write command, and an extended command, citing figure 4, the abstract, and paragraph 29. Applicant is unable to find anything in the cited portions of Ryan that disclose command flag bits or any other bits that indicate one of an activate command, a read/write command, and an extended command.

Regarding claim 4, the Examiner asserts that Ryan discloses that the memory control packet specifies a memory row, a memory row address, a memory bank address, and a device identification mask if the memory control packet is the activate command, citing figures 3 and 4 and the signals on element 154 of figure 4. Element 154 is a bus carrying SDRAM command/control lines to the non-packet based main memory and therefore discloses nothing about what is specified by the packets. Paragraph 28. The cited portion does not disclose anything about what is specified by the packets nor do they disclose a device identification mask in the packets or elsewhere.

Regarding claim 5, the Examiner asserts that Ryan discloses that the memory control packet specifies a memory row, a memory column address, and a memory bank address, if the memory control packet is the read/write command, citing figures 3 and 4 and the signals on element 154 of figure 4. Element 154 is a bus carrying SDRAM command/control lines to the non-packet based main memory and therefore discloses nothing about what is specified by the packets. Paragraph 28. Ryan discloses a device that receives RDRAM protocol packets that provide a memory row and a memory bank addresses in a ROWx packet and a memory column address in a separate COLx packet. Paragraphs 31-33. The is unlike the claimed device in which a memory row, a memory column address, and a memory bank address are all in a single memory control packet.

Regarding claim 6, the Examiner asserts that Ryan discloses that, if the memory control packet is the extended command, the memory control packet includes extended flag bits that indicate that the memory control packet is one of a retire with mask command, a pre-charge command, and a service command, citing paragraphs 29 and 32-36. Applicant can find nothing in the cited portions that discloses the recited elements of the claim.

Regarding claim 7, the Examiner asserts that Ryan discloses that the memory control packet specifies a memory row, and a byte mask, if the memory control packet is the retire with mask command, citing paragraphs 33-35. Applicant can find nothing in the cited portions that discloses the recited elements of the claim.

Regarding claim 9, the Examiner asserts that Ryan discloses that the memory control packet specifies a memory row, an operation, and one of a broadcast flag and a memory bank address, if the memory control packet is the service command, citing paragraphs 29-35. Applicant can find nothing in the cited portions that discloses the recited elements of the claim.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-23 under 35 U.S.C. § 102(e) as being anticipated by either Ryan (US 2001/0042163 A1) or Ryan (US 6,449, 679 B2).

The Examiner rejects claims 1-23 under 35 U.S.C. § 102(a) as being anticipated by "SDRAM to Direct RDRAM" (the presentation).

Applicant notes that the presentation is undated, that the reference was cited under "Other Publications" in the Ryan patent as an undated reference, and that the Examiner has provided nothing to indicate that the presentation was published prior to the applicant's filing date. Applicant respectfully submits that the Examiner has the burden of establishing a date of publication to make a *prima facie* case of anticipation under 35 U.S.C. § 102(a).

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-23 under 35 U.S.C. § 102(a) as being anticipated by the presentation.

The Examiner rejects claims 1-23 under 35 U.S.C. § 103(a) as being unpatentable over Ingenio et al. (US 6,041,361).

The Examiner asserts that it would obvious to have modified the input and output interfaces of the memory control device taught by Ingenio to accommodate any system memory controller/memory device combination desired or required.

In responding to Applicant's previously presented argument, the Examiner states, "The reference is open-ended and teaches making an otherwise incompatible memory connection." The Examiner appears to argue that the generalized disclosure of Ingenio makes obvious every particular invention for making an otherwise incompatible memory connection. Clearly this is not what the Examiner intended to say since the Examiner allowed Ryan's claims to a device that connects a memory controller using packet based RDRAM protocol to connect to memory devices that use SDRAM protocol. Applicant respectfully submits that applicant's claims to a device that connects a memory controller using memory control packets, as defined by the specification, to connect to memory devices that use SDRAM protocol should be likewise allowable over Ingenio.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-23 under 35 U.S.C. § 103(a) as being unpatentable over Ingenio.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Dated: March 4, 2004

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